10-14-03

Ser. No.: 09/771,229

Page 1 of 4

Attorney Docket No.: FUJS 13.045A (100794-10736)

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Inventor

Takanori IWAMATSU Hiroyuki KIYANAGI

Serial No.

Filed

09/771,229

January 26, 2001

Title

**CLOCK PHASE DETECTING CIRCUIT AND CLOCK** REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT

Examiner

Young Toi Tse

Group Art Unit

2634

Mail Stop Petitions Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

OCT 2 0 2003

Technology Center 2600

#### PETITION UNDER 37 CFR 1.181(A) REQUESTING WITHDRAWAL OF HOLDING OF ABANDONMENT

To the Commissioner for Patents:

Applicant received a Notice of Abandonment, a copy of which is enclosed, mailed on September 30, 2003. The Notice of Abandonment indicated that the above-identified application was abandoned due to Applicants' failure to timely reply to an Office Action mailed on February 26, 2003. However, Applicants respectfully submit that a timely reply was made on August 26, 2003, as attested to by Applicants' undersigned attorney of record in a declaration enclosed herewith.

> Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Filed by Express Mail

Receipt No. 2298018466245

on Des - 13 - 03

Patricia Muir

Ser. No.: 09/771,229 Page 2 of 4

Applicants also enclose copies of the documents mailed on August 26, 2003 in

Applicants' timely reply, including a Response to Office Action, a Petition for a three-month

extension of time, and a revised Figure 14. Applicants further attach a copy of a return receipt

postcard indicating receipt of these documents by the Office of Initial Patent Examination on

August 26, 2003.

Accordingly, Applicants respectfully request that the holding of abandonment be

withdrawn, that the Response of August 26, 2003 be considered and that the application be

allowed.

It is believed that no fee is due with this petition. However, if any fee is due with this

paper, the Commissioner is hereby authorized to charge such fee on Deposit Account No. 50-

1290.

Any inquiries regarding the current petition may be directed to Applicant's undersigned

attorney of record, who may be reached directly by telephone at (212)940-8729.

Respectfully submitted,

Thomas J. Bean

Reg. No. 44,528

Attorney for Applicant

Katten Muchin Zavis Rosenman 575 Madison Avenue New York, NY 10022-2585

Phone: (212)940-8800

Docket No.: FUJS 13.045A (100794-10736)

Ser. No.: 09/771,229

Page 3 of 4

Attorney Docket No.: FUJS 13.045A (100794-10736)

Inventor

Takanori IWAMATSU Hiroyuki KIYANAGI

Serial No.

09/771,229

Filed

January 26, 2001

Title



CLOCK PHASE DETECTING CIRCUIT AND CLOCK REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT

Examiner

Young Toi Tse

Group Art Unit

2634

October 10, 2003

RECEIVED

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

OCT 2 0 2003

# STATEMENT OF THOMAS J. BEAN IN SUPPORT OF PETITION UNDER 37 CFR 1.181(A)

Technology Center 2600

I, Thomas J. Bean (Reg. No. 44,528), hereby declare that:

- 1. I am an attorney of record for the above-identified patent application.
- 2. I prepared a Response to Office Action, a Petition for a three-month extension of time, and a revision to Figure 14 in response to an Office Action mailed January 31, 2003 in regard to the above-referenced application.
- 3. Upon information and belief, the Response to Office Action, Petition for a three-month extension of time, and revision of Figure 14 were timely mailed by Express Mail on August 26, 2003, and true copies of these documents are provided with this Statement.
- 4. Upon information and belief, the number of the Express Mail mailing label EV 332275680US was placed on the first pages of the Petition for extension of time and Response mailed on August 26, 2003.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Filed by Express Mail

Receipt No. £2980184662 45

on 6-4 - 13 - 07
pursuant to 37 C.F.R. 1.10.

Patricia Muir

Ser. No.: 09/771,229 Page 4 of 4

5. Upon information and belief, a postcard was returned to Applicants' representative by the Office of Initial Patent Examination, indicating receipt of the above-listed documents on August 26, 2003.

6. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date:

10 10 03

Thomas B Bean

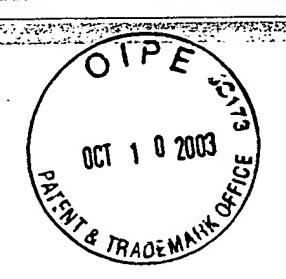


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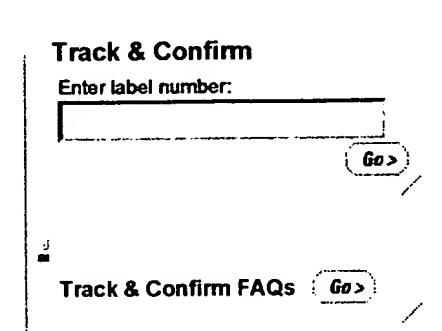
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09/771,229 01/26/2001 Takanori Iwamatsu FUJS 13.045A 6938  26304 7590 09/30/2003  KATTEN MUCHIN ZAVIS ROSENMAN 575 MADISON AVENUE NEW YORK, NY 10022-2585  ART UNIT PAPER NUMBER  2634  DATE MAILED: 09/30/2003						
26304 7590 09/30/2003  KATTEN MUCHIN ZAVIS ROSENMAN 575 MADISON AVENUE NEW YORK, NY 10022-2585  ART UNIT PAPER NUMBER  2634  DATE MAILED: 09/30/2003	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
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Please find below and/or attached an Office communication concerning this application or proceeding.



# Notice of Abandonment

Application No.	Applicant(s)		
09/771,229	IWAMATSU ET AL.		
Examiner	Art Unit	-	
YOUNG T. TSE	2634		

	YOUNG I. ISE	2634	_
The MAILING DATE of this communication ap	pears on the cover sheet	with the correspondence	address-
This application is abandoned in view of:			
<ol> <li>Applicant's failure to timely file a proper reply to the Off         <ul> <li>(a)  A reply was received on (with a Certificate of period for reply (including a total extension of time of time of time)</li> </ul> </li> </ol>	Mailing or Transmission da	ted), which is after th	ne expiration of the
(b) A proposed reply was received on, but it does	s not constitute a proper re	oly under 37 CFR 1.113 (a) t	o the final rejection.
(A proper reply under 37 CFR 1.113 to a final reject application in condition for allowance; (2) a timely fil Continued Examination (RCE) in compliance with 3	ed Notice of Appeal (with ap		
(c) A reply was received on but it does not constitute final rejection. See 37 CFR 1.85(a) and 1.111. (Se			eply, to the non-
(d) No reply has been received.		:	
2.  Applicant's failure to timely pay the required issue fee a from the mailing date of the Notice of Allowance (PTOL	-85).		
(a) The issue fee and publication fee, if applicable, w), which is after the expiration of the statutory Allowance (PTOL-85).			
(b) The submitted fee of \$ is insufficient. A balar	ice of \$ is due.		
The issue fee required by 37 CFR 1.18 is \$	The publication fee, if requ	uired by 37 CFR 1.18(d), is \$	S
(c) The issue fee and publication fee, if applicable, has	not been received.		
<ol> <li>Applicant's failure to timely file corrected drawings as re Allowability (PTO-37).</li> </ol>	quired by, and within the th	ree-month period set in, the	Notice of
(a) Proposed corrected drawings were received on after the expiration of the period for reply.	(with a Certificate of Ma	ling or Transmission dated _	), which is
(b) No corrected drawings have been received.	•		
4. The letter of express abandonment which is signed by the applicants.	the attorney or agent of rec	ord, the assignee of the entir	re interest, or all of
5. The letter of express abandonment which is signed by 1.34(a)) upon the filing of a continuing application.	an attorney or agent (acting	in a representative capacity	under 37 CFR
6.  The decision by the Board of Patent Appeals and Interform of the decision has expired and there are no allowed cl		and because the period for s	seeking court review
7. The reason(s) below:	· .		
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# THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor

Takanori IWAMATSU

Hiroyuki KIYANAGI

RECEIVED

Serial No.

09/771,229

OCT 2 0 2003

Filed

January 26, 2001

Technology Center 2600

Title

**CLOCK PHASE DETECTING CIRCUIT AND** 

**CLOCK REGENERATING CIRCUIT EACH** 

ARRANGED IN RECEIVING UNIT OF MULTIPLEX

**RADIO EQUIPMENT** 

Examiner

Young Toi Tse

Group Art Unit

2634

August 26, 2003

Mail Stop Reissue Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

# AMENDMENT UNDER 37 C.F.R. § 1.173(b)

Sir:

Applicant hereby petitions for a three-month extension, a petition pursuant to 37

C.F.R. §1.136(a) and authorization to charge the requisite fee being enclosed.

In response to the Office Action dated February 26, 2003, please amend the

subject application as follows:

Any fee due with this paper may be charged to Deposit Account No. 50-1290. Filed by Express Mail

Receipt No. 2 33227568 45 on AUGUST 26, 2003

By

pursuant to 37 C.F.R. 1.10.

Patricia Muir

#### IN THE SPECIFICATION

# Please amend the paragraph beginning at column 2, line 11 as follows:

The clock regenerating circuit 75 regenerates A/D conversion clocks, of which the timing at which the [A/ID] A/D converters 72 and 73 execute an A/D conversion (the so-called eye pattern in fully open state) matches the phase, from a received signal to be detected by the orthogonal detecting unit 75 and then supplies them respectively to the A/D converters 72 and 73. The clock regenerating circuit 75 is formed of a square detecting unit 76, a filer 77, and a PLL circuit 78. The PLL circuit 78 is formed of a phase detector (PD) 79, a loop filter 80, an amplifier 81 and an oscillating unit 82.

# Please amend the paragraph beginning at column 2, line 45 as follows:

The clock regenerating circuit 83 proposed by Japanese Patent Laid-open Publication (Tokukaisyo) No. 63-215235 as shown in FIG. 61, is formed of a phase deviation detection unit 831, [a] an infinite phase shifter 832, and an oscillating unit 833. Numeral 81 represents a demodulating unit which demodulates a received signal and 82 represents a data regenerating unit that regenerates a demodulated signal (data) from the demodulating unit. The data regenerating unit 82 consists of an equalizer (EQL) 821 that subjects a demodulated signal to an equalizing process and an identifier (A/D converter) that identifies and encodes (digitalizes) the level of the demodulated signal processed by the equalizer.

# Please amend the paragraph beginning at column 4, line 13 as follows:

According to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying unit for identifying a signal at a predetermined identification level, the signal being obtained by demodulating a multi-level orthogonal modulated signal and an equalizing circuit for subjecting the demodulated signal to an equalizing process, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit an then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock regenerating unit for regenerating the signal identification clock based on a signal before the multilevel orthogonal modulated signal is detected[;], a phase adjusting unit for adjusting the phase of a clock from the clock regenerating unit and then supplying the phase-adjusted clock to the identifying circuit[;], and a clockphase detecting unit for detecting a phase component of the signal identification clock based on input/output signals of the equalizing circuit and then supplying the result as the phase adjustment control signal to the phase adjusting unit.

# Please amend the paragraph beginning at column 4, line 50 as follows:

Furthermore, according to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying circuit for identifying a signal at a predetermined identification level, the signal being obtained by demodulating a multilevel orthogonal modulating signal and an equalizing circuit for subjecting the demodulated signal to an equalizing process, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit and then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock phase detecting unit for detecting a phase component of the

signal identification clock based on [input/output] input/output signals of the equalizing circuit[;], a loop filter unit for integrating the output from the clock phase detecting unit[;], and an oscillating unit for producing a signal identification clock for the identifying circuit to the identifying circuit, in response to as a control input the output from the loop filter unit.

#### Please amend the paragraph beginning at column 6, line 6 as follows:

According to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying circuit for identifying a signal at a predetermined identification level, the signal being obtained by demodulating a multilevel orthogonal modulated signal, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit and then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock phase detecting circuit for detecting a phase component of the signal identification clock based on clock phase difference information supplied to the identifying circuit and signal error differential information obtained by the identifying circuit which supplies it to the clock regenerating circuit[;], a loop filter unit for integrating the output from the clock phase detecting unit[;], and an oscillating circuit for producing a signal identification clock for the identifying circuit to the identifying circuit, in response to the output as a control input from the loop filter circuit.

### Please amend the paragraph beginning at column 25, line 50 as follows:

In the clock regenerating circuit 35A having the above-mentioned configuration, like the configuration shown in FIGS. 7 and 9, the phase component detecting unit 26A

arranged corresponding to the channel (Ich) identifying unit 23 detects the phase shift of and A/D conversion clock based on an Ich signal while the phase component detecting unit 26B arranged corresponding to the channel (Qch) identifying unit 24 detects the phase shift of an A/D conversion clock based on a Qch signal. The integrator [27] 27A averages the phase shift of an A/D conversion clock to supply as a phase adjustment and control signal for the phase shifter 28A to the phase shifter 28A while the integrator [27] 27B averages the phase shift of an [A/ID] A/D conversion clock to supply as a phase adjustment and control signal for the phase shifter 28B to the phase shifter 28B. As a result, the phase shifters 28A and 28B adjust independently the phase of the A/D conversion clock regenerated in the clock regenerating unit 29 and supply it respectively to the identifying units 23 and 34.

# Please amend the paragraph beginning at column 26, line 38 as follows:

In the inclination judging unit 30A having the above-mentioned configuration, the FF circuit 306, for example, as shown in FIG. 16, latches the current Ich signal (at the time"0") and the past Ich signal (at the time "-T/2") delayed by the time T/s by the [FE] FF circuit 305 and then outputs them to the comparing unit 307 according to the basic clocks from the frequency divider 36.

# Please amend the paragraph beginning at column 34, line 53 as follows:

Hence the phase shift of an [A/ID] A/D conversion clock for the A/D converters 23A, 23B, and 24 can be adjusted automatically and with high accuracy to supply to the identifying units (A/D converters) 23A, 23B, and 24.

#### IN THE CLAIMS

8. (twice amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit comprises:

an error detecting unit for detecting an input signal to output signal error of said [equilizing] equalizing circuit;

a signal inclination detecting unit for detecting the inclination is said demodulated signal;

a clock phase calculating unit for detecting the phase component of said signal identification clock by calculating based on the respective outputs from said error detecting unit and said signal inclination detecting unit;

a specific signal judging unit for judging whether a specific signal exists; and

a gating unit for [producting] <u>producing</u> the phase component of said signal identification clock obtained by said clock phase calculating unit when said specific signal judging unit judges that said specific signal exists.

14. (twice amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 8, wherein said specific signal judging unit includes plural signal judging units that judge plural kinds of specific signals, and further comprising a selecting unit arranged between said [specific signal judging unit] plural signal judging units and said [gate] gating unit, for selecting decision results from said plural signal judging units.

15. – 46. (canceled)

#### REMARKS

An Office Action was mailed on February 26, 2003. Claims 1-47 are pending in the present application. With this Response, Applicants amend the specification, amend FIG. 14, cancel claims 15-46, and amend claims 8 and 14. No new matter is introduced.

#### REJECTION UNDER 35 U.S.C. § 251

Claims 1 – 47 are rejected under 35 U.S.C. § 251 as being based on a defective reissue application. Applicants' cancel claims 15 – 46, and respectfully traverse this rejection.

35 U.S.C. § 251 provides in the following basis for reissuing a patent:

Whenever any patent is, through error without any deceptive intention, deemed wholly or partly inoperative or invalid, by reason of a defective specification or drawing, or by reason of the patentee claiming more or less than he had a right to claim in the patent ...

(Emphasis added)

On April 17, 2001, in response to a Notice to File Missing Parts mailed on March 7, 2001, Applicants mailed a properly-formed re-issue application declaration by the inventors asserting a belief that the underlying issued patent (U.S. Patent No. 5,867,542) was wholly or partly inoperative or invalid, by reason of the patentee claiming more or less than he had the right to claim by failing to provide a generic claim to the various embodiments disclosed in the original patent.

The Examiner asserts that a failure to timely file a divisional application has been held as not considered to be an error causing a patent granted on elected to claims to be partially inoperative by reason of claiming less than Applicants had a right to claims (citing In re Watkinson, 900 F.2d 230, 14, U.S.P.Q.2d 1407 (Fed. Cir. 1990), In re Orita,

550 F.2d 1277, 193 U.S.P.Q. 145 (CCPA 1977) and <u>In re Mead</u>, 581 F.2d 251, 198 U.S.P.Q. 412 (CCPA 1978) for what has become known as "the <u>Orita</u> doctrine").

In In re Doyle, the Federal Circuit clarified the limitations of the Orita doctrine by affirming that "the so-called Orita doctrine therefore precludes a reissue applicant from obtaining substantially identical claims to those of nonelected groups identified in an examiner's restriction requirement when such claims could not have been prosecuted in the application from which they were restricted." (In re Doyle, 293. F.3d 1355, U.S.P.Q.2d 1161 (Fed. Cir. 2002), emphasis added). Applicants acknowledge this affirmation, and cancel claims 15 – 46, which Applicants described in their Preliminary Amendment of January 26, 2001 as being substantially similar to restricted claims 15 – 46 of the original parent application, "with only the slightest non-substantive changes".

However, Applicants respectfully submit that the Orita doctrine is not applicable to claims 1 – 14 and 47 of the present application. Claims 1 – 14 and 47 are neither identical nor substantially similar to nonelected claims 15 – 46 of the original parent application. In addition, as claims 1 – 14 are substantially similar to elected claims 1 – 14 in the original parent application, and claim 47 represents a linking claim that could have been prosecuted together with the elected claim group, each of claims 1 – 14 and 47 could have been prosecuted in the original patent application.

In <u>Doyle</u>, the Federal Circuit was presented with facts quite similar to those associated with the present application. Doyle received a restriction requirement in an original parent application, and elected one of nine identified claim groups for prosecution, canceling claims in the other restricted groups. Doyle failed to file divisional applications during the pendency of the original patent application. Doyle timely filed a request for broadening reissue with "linking" genus claims, and conceded that these

genus claims read on but were broader than any of the non-elected claims. On appeal, the Board of Patent Appeals and Interferences applying the Orita doctrine held Doyle's reissue declaration to be invalid.

However, in <u>Doyle</u>, the Federal Circuit <u>overturned the Board's holding</u>, holding that Doyle's declaration of failure to claim all that he was entitled to by failing to include genus claims that read on but are broader than the claims of non-elected groups was proper under 35 U.S.C. § 251. The court's opinion included the following rationale:

The linking claims here are obviously not of substantially similar scope as the nonelected species claims - they are quite significantly broader. More importantly, they could have been asserted along with the elected group because they read on the species of the elected group. Indeed, had Dr. Doyle not inadvertently neglected to assert the linking claims in his prosecution of the elected group, and had those claims been allowed, the examiner would have been required to lift the restriction requirement as to the other groups linked by the new claims and allow prosecution of those other groups. The MPEP expressly provides that "[I]f a linking claim is allowed, the examiner <u>must</u> examine the claims to the nonelected inventions that are linked to the elected invention by such allowed linking claim." MPEP § 809.04 (emphases added). Viewed in this light, Dr. Doyle's failure to asset the linking genus claims truly was an error in the issued patent. It was not, as in In re Orita, merely an error pertaining to the prosecution (or lack thereof) of other, divisional applications directed towards the nonelected groups.

(Additional emphasis added)

Accordingly, Applicants respectfully submit that Applicants' reissue declaration as to claims 1-14 and 47 is not defective under the holding of <u>Doyle</u>, and respectfully request that this rejection be withdrawn.

#### **OBJECTION TO DRAWING**

FIG. 14 objected to under 37 C.F.R. § 1.84(p)(5) for failing to include reference sign 307, which is mentioned in the specification at column 26, line 34. Applicants attach clean and marked-up versions of a proposed amended FIG. 14 to include reference sign

307. Accordingly, Applicants respectfully request approval of the proposed changes, and withdrawal of the drawing objection.

#### **OBJECTIONS TO SPECIFICATION**

The specification is objected to for a variety of informalities at columns 2, 4, 6, 23, 26 and 34. Applicants amend the specification to address these informalities, and respectfully request that the objection be withdrawn. No new matter is added.

#### **OBJECTIONS TO CLAIMS**

Claims 3 – 28, 30 – 32, 34 – 39 and 41 – 46 are objected to for various informalities. Applicants cancel claims 3 – 28, 30 – 32, 34 – 39 and 41 – 46 without prejudice or disclaimer, and respectfully request that the objections be withdrawn. Claims 8 and 14 are amended to correct these informalities, and to correct several typographical errors. Applicants request clarification as to the Examiner's objection to claim 8 which was unclear to Applicants, and respectfully request that all claim objections be withdrawn.

#### REJECTIONS UNDER 35 U.S.C. § 112

Claims 16-21, 23-28, 34-39 and 41-46 are rejected under the first paragraph of 35 U.S.C. 112 as containing subject matter not described in the specification in such a way to enable one skilled in the art to make or use the disclosed invention.

Claims 19, 24-27, 29-39 and 43-45 are rejected under the second paragraph of 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim that which the inventors consider to be their invention. Applicants cancel claims 16-21, 23-28, 29-39 and 41-46 without prejudice or disclaimer, and respectfully request that the rejections be withdrawn.

#### REJECTIONS UNDER 35 U.S.C. §§ 102, 103

Claims 29 – 32, 40 – 42, 44 and 47 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,317,602 to Onoda et al. Claims 33, 35 and 37 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,438,591 to Oie et al. Claims 29 – 30, 40 – 42, and 47 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,535,252 to Kobayashi. Applicants cancel claims 29 – 33, 35, 37, 40 – 42 and 44 without prejudice or disclaimer, and respectfully traverse the rejections as to claim 47.

In independent claim 47, Applicants disclose a receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising: a) an identifying circuit for identifying a demodulated signal at a predetermined identification level, the demodulated signal obtained by demodulating a multilevel orthogonal modulated signal, b) a clock regenerating circuit for regenerating a signal identification clock and supplying the regenerated signal identification clock to the identifying circuit, and c) a clock phase detecting section for detecting a phase component of the signal identification clock based on clock-phase-detecting composite input information including one of: i) a combination of a demodulated signal and an equalized demodulated signal, and ii) a combination of clock phase information to be supplied to the identifying circuit and signal error information obtained by the identifying circuit, and for then supplying the phase component to the clock regenerating circuit. The clock phase detecting section further includes: a) a difference detecting unit, responsive to the receipt of the composite input information, for detecting any one of: I) difference information between the demodulated signal and the equalized demodulated signal, and II) a combination of clock phase difference information and signal error differential information, and b) a clock phase

calculating unit for calculating the phase component of the signal identification clock based on the output from the difference detecting unit.

Onoda discloses a QPSK base-band delayed detector (see, e.g., FIG. 5 of Onoda). The detector of Onoda includes A/D converters 57, 58 for identifying and converting analog signals into digital signals and bit timing recovery (BTR) circuit 1 including phase comparison result detection unit 2 for detecting a phase component of the digital signals generated by converter 57, 58, and a digital PLL 3 for outputting a clock signal of appropriate phase. Unlike Applicants' claimed invention, however, Onoda fails to disclose that detection unit detects either of difference information between the demodulated signal and the equalized demodulated signal or a combination of clock phase difference information and signal error differential information.

Kobayashi discloses a DQPSK clock synchronization circuit (see, e.g., FIG. 2 of Kobayashi). The circuit of Kobayashi includes A/D converters 41, 42 for detecting and converting analog signals into digital signals, phase detector circuits 43, 45, 46 and 47 for detecting a phase error in the digital signals, and clock reproducer 48 for generating a clock signal m for A/D converters 41, 42. As in the case of Onoda, in sharp contrast to Applicants' claimed invention, Kobayashi fails to disclose that detector circuits 43, 45, 46 and 47 detect either of difference information between the demodulated signal and the equalized demodulated signal or a combination of clock phase difference information and signal error differential information.

Accordingly, Applicants respectfully submit that claim 47 is not anticipated by either of Onoda and Kobayashi, and is therefore allowable

#### **CONCLUSION**

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that 1 – 14 and 47, which include independent claims 1, 2, 8 and 47, and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Respectfully submitted,

Thomas J. Bean Reg. No. 44,528

**CUSTOMER NUMBER 026304** 

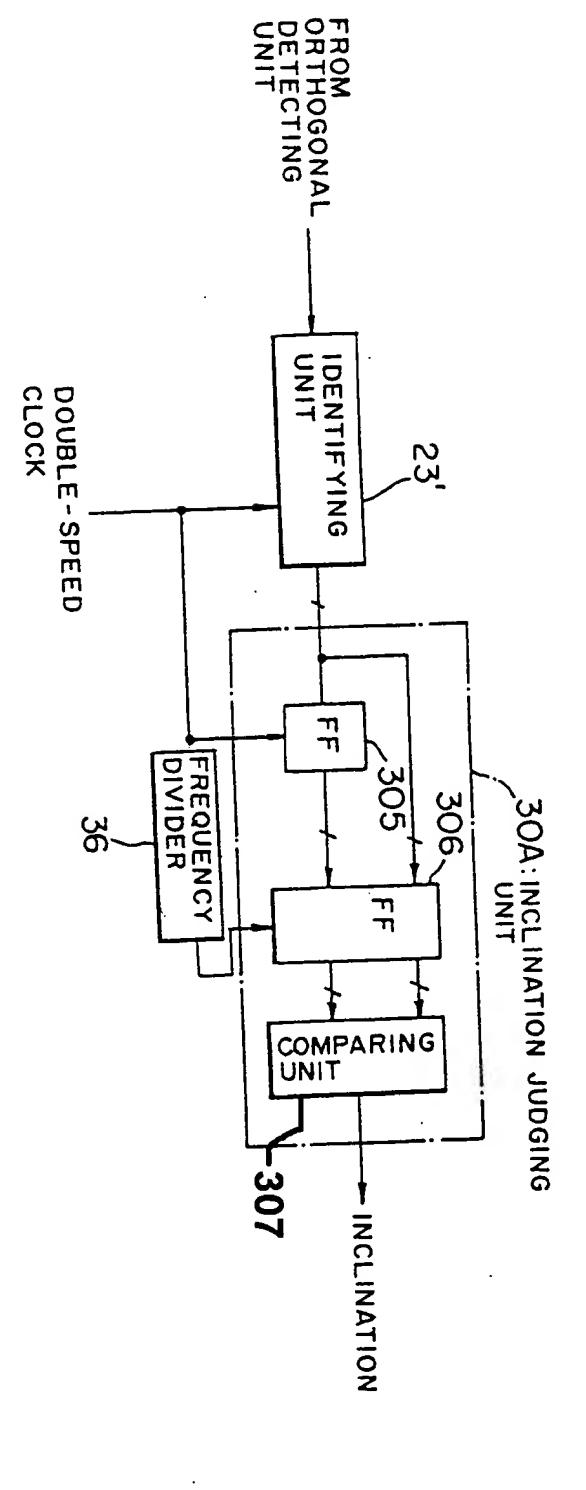
KATTEN MUCHIN ZAVIS ROSENMAN 575 MADISON AVENUE NEW YORK, NEW YORK 10022-2585

PHONE: (212) 940-8800/FAX: (212) 940-8776 DOCKET No.: FUJS 13.045A (100794-10736)

ENCLOSURE: Amended FIG. 14



F | G. 14



# THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor

Takanori IWAMATSU

Hiroyuki KIYANAGI

Serial No.

09/771,229

Filed

January 26, 2001

Title

CLOCK PHASE DETECTING CIRCUIT AND CLOCK

REGENERATING CIRCUIT EACH ARRANGED IN

RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT

Examiner

Young Toi Tse

Group Art Unit

2634

August 26, 2003

RECEIVED

OCT 2 0 2003

Mail Stop Reissue Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

Technology Center 2600

# PETITION FOR EXTENSION OF TIME

Sir:

Applicant requests that the time for taking action in this case be extended pursuant to 37 CFR 1.136(a) for:

( ) one month

(X) three months

( ) two months

( ) four months

The fee set in 37 CFR 1.17 for the extension of time is \$930.

() Fee enclosed. Please charge any additional fee required for this extension of time to Deposit Account No. 50-1290. A duplicate copy of this paper is enclosed.

Any fee due with this paper may be charged to Deposit Account No. 50-1290. Filed by Express Mail

Receipt No. 8/33227 58 80 45

on AUGUST 26, 2002-

pursuant to 37 C.F.R. 1.10.

Patricia Muir

(xx) Charge fee to Deposit Account No. 50-1290. A duplicate copy of this paper is enclosed.
( ) Applicant is a small entity entitled to pay reduced fees in this application.
A verified small entity statement:

( ) has been filed ( ) is enclosed.

Also enclosed is a:
( X) Response ( ) Notice of Appeal ( ) Appeal Brief
( ) Sub Power of Attorney
Change of Correspondence Address

Respectfully submitted,

Thomas J. Bean Reg. No. 44,528

#### CUSTOMER NUMBER 026304

KATTEN MUCHIN ZAVIS ROSENMAN 575 Madison Avenue New York, NY 10022-2585 (212) 940-8703

Docket No.: FUJS 13.045A (100794-10736)

TJB:pm